WHAT IS CLAIMED IS:

1. A diode comprising:

a semiconductor substrate of either of first or second conductivity type;

first and second stripe diffusion regions which are of said first conductivity type and a second conductivity type, respectively, alternately arranged at a regular interval in a surface portion of said semiconductor substrate, longitudinal sides of said first and second stripe diffusion regions being arranged so as to face each other;

first electrodes being supported by said semiconductor substrate and connected to said first and second diffusion regions, respectively; and

a second electrode covering through an insulation layer neighboring ends of said first and second diffusion regions, a potential of said second electrode being equalized to a potential of the first electrode connected to either one of said first and second diffusion regions of which conductivity type is different from that of said semiconductor substrate.

2. The diode as claimed in claim 1, wherein said second electrode is formed integrally with said first electrode connected to the either one of said first and second diffusion regions of which conductivity type is different from that of said semiconductor substrate.

3. The diode as claimed in claim 1, wherein said insulation layer comprises localized oxidation of silicon, and said second electrode comprises polycrystalline silicon.

4. A diode comprising:

a semiconductor substrate of either of first or second conductivity type;

first and second stripe diffusion regions which are of said first conductivity type and a second conductivity type, respectively, alternately arranged at a regular interval in a surface portion of said semiconductor substrate, longitudinal sides of said first and second stripe diffusion regions being arranged so as to face each other;

first and second stripe electrodes formed above said first and second diffusion regions along said longitudinal sides, connected to said first and second diffusion regions, respectively; and

first and second lead wire electrodes having widths which are shorter than longitudinal sides of said first and second stripe electrodes, connected to said first and second stripe electrodes expect at first and second ends of said first and second stripe electrodes, respectively.

5. The diode as claimed in claim 4, wherein said first and second lead wire electrodes are connected to said first and second stripe electrode at middle portions of said first and second electrodes regarding said longitudinal sides, respectively.

6. The diode as claimed in claim 4, further comprising:

an insulation layer between said first and second stripe electrodes and said first and second lead wire electrodes,

wherein said first and second stripe electrodes are arranged as lower layers, said first and second lead wire

electrodes are arranged as upper layers, and said first and second stripe electrodes and said first and second lead wire electrodes are connected through via-holes formed in said insulation layer, respectively.

7. The diode as claimed in claim 6, wherein said first and second lead wire electrodes have first and second comb shapes of which first and second teeth intersect said first and second stripe electrodes, respectively, teeth of first and second comb shapes interlace with each other, and wherein said via-holes are arranged at intersections of said first and second stripe electrodes and teeth of said first and second comb shapes, respectively.

8. A diode comprising:

a substrate of a first conductivity type;

first and second stripe diffusion regions which are said first conductivity type and a second conductivity type, respectively, alternately arranged at a regular interval in a surface layer of said semiconductor substrate, longitudinal sides of said first and second stripe diffusion regions being arranged so as to face each other;

first and second stripe electrodes above said first and second diffusion regions along said longitudinal sides, connected to said first and second diffusion regions, respectively; and

surge current concentration suppressing means for suppressing concentration of surge current at neighboring ends of said first and second stripe diffusion regions.

9. The diode as claimed in claim 8, wherein said surge

current concentration suppressing means comprises:

first and second lead wire electrodes having widths which are shorter than longitudinal sides of said first and second stripe electrodes, connected to said first and second stripe electrodes expect at first and second ends of said first and second stripe electrodes, respectively.

10. The diode as claimed in claim 8, wherein said surge current concentration suppressing means comprises:

chamfered portions formed at the neighboring ends of said first and second stripe diffusion regions by chamfering end edges of said first and second stripe diffusion regions.

11. The diode as claimed in claim 10, wherein said chamfered portion is a semicircle portion.

12. The diode as claimed in claim 8, wherein said surge current concentration suppressing means comprises:

said second stripe diffusion region of the second conductivity type different from the first conductivity type of said semiconductor substrate, having a longitudinal length greater than said first stripe diffusion region so that end portions of said second stripe diffusion region extend beyond those of said first stripe diffusion region in a longitudinal direction.

13. The diode as claimed in claim 8, wherein said surge current concentration suppressing means comprises:

a region formed at the end of said second stripe diffusion region of the second conductivity type different from the first conductivity type of said semiconductor substrate, said region having a diffusion concentration which

is lower than said second stripe diffusion region.

14. The diode as claimed in claim 8, wherein said surge current concentration suppressing means comprises:

a third electrode covering neighboring ends of said first and second stripe diffusion regions;

an insulation layer for insulating at least said first stripe diffusion region from said third electrode; and

electrical connection means for electrically connecting said third electrode to said second stripe diffusion region.

15. The diode as claimed in claim 14, wherein said electrical connection means connects said third electrode to said second stripe diffusion region by integrally forming said third electrode and said second stripe electrode connected to said second stripe diffusion region.

16. The diode as claimed in claim 14, wherein said insulation layer comprises localized oxidation of silicon, and said third electrode comprises polycrystalline silicon.

17. The diode as claimed in claim 8, wherein said surge current concentration suppressing means comprises:

first and second contacts for providing first electrical connection between an intermediate portion of said first stripe diffusion region and said first stripe electrode and second electrical connection between an intermediate portion of said second stripe diffusion region and said second stripe electrode, respectively.

18. The diode as claimed in claim 8, wherein said surge current concentration suppressing means comprises:

first and second lead wire electrodes connected to

middle portions of said first and second stripe electrodes, respectively.

19. A diode comprising:

a semiconductor substrate;

an insulation protection film on said semiconductor substrate having three openings arranged in a predetermined direction, said three openings being spaced by two bridge portions having the same width in said predetermined direction;

a first impurity diffusion region of a first conductivity type disposed in a surface layer of said semiconductor substrate under center one of said three openings;

second impurity diffusion regions of a second conductivity type disposed in said surface layer under outer two of said openings, respectively;

first and second PN junction regions in said surface layer between said first impurity diffusion region and said second impurity diffusion regions, said first and second PN junction regions being covered with said bridge portions and having PN junction widths depending on said bridge portions, said insulation protection film having a melting point higher than the PN junction regions;

a first electrode on said insulation protection film connecting to said first impurity diffusion region through said opening; and

a second electrode on said insulation protection film connecting said second impurity diffusion regions through

said openings.

20. The diode as claimed in claim 19, wherein each of said openings has a rectangle shape of which longitudinal sides are defined by said bridge portions of said insulation protection film.

21. The diode as claimed in claim 20, wherein said longitudinal sides of said rectangle shape of said center one of said openings are different in length from said longitudinal sides of said outer two of said openings.

22. The diode as claimed in claim 20, wherein said openings of the insulation protection film have round portions or chamfered portions at its ends so that corners of said rectangle shape are rounded or chamfered.

23. The diode as claimed in claim 20, further comprising low impurity concentration diffusion regions in said surface layer covering end edge portions of at least one of said first and second impurity diffusion regions, wherein an impurity concentration of said low impurity concentration diffusion region is lower than an impurity concentration of said one of said first and second impurity diffusion regions, and wherein a conductivity type of said low impurity concentration diffusion region is the same as the conductivity type of said one of said first and second high impurity concentration diffusion regions.

24. The diode as claimed in claim 20, wherein said first and second electrodes have contact areas within said openings for contacting with said first and second impurity diffusion regions, a distance ($L_y$) between the transverse sides of said

openings and contact areas is greater than a distance ($L_x$) between the longitudinal sides of said openings and contact areas.

25. The diode as claimed in claim 19, wherein said three openings in said insulation protection film are coaxially arranged.

26. The diode as claimed in claim 19, wherein said first electrode comprises a first lower layer electrode partially covering said first impurity concentration diffusion region inside said center one of said three openings, and said second electrode comprises second lower layer electrodes partially covering said second impurity diffusion region inside said outer two of said three openings, said diode further comprising an intermediate insulation layer on said first and second lower layer electrodes, said intermediate insulation layer having a first lower layer electrode opening at the corresponding position of said first lower layer electrode and second lower layer electrode openings at the corresponding positions of said second lower layer electrodes, wherein said first electrode further comprises a first upper layer electrode connected to said first lower layer electrode through said first lower layer electrode opening, and said second electrode further comprises a second upper layer electrode connected to said second lower layer electrodes through said second lower layer electrode openings.

27. The diode as claimed in claim 26, wherein widths of said first and second upper layer electrodes is greater than widths of said first and second lower layer electrodes,

respectively.

28. The diode as claimed in claim 26, further comprising a protection film on said first and second upper layer electrodes having first and second openings, wherein a first pad is formed by a part of said first upper layer electrode exposed through said openings and second pad is formed by a part of said second upper layer electrode exposed through said openings, and said first and second pads are provided on locations where three openings are put therebetween, and widths of said first and second upper layer electrodes increase as distances to said first and second pads decrease, respectively.

29. The diode as claimed in claim 19, further comprising:

a third impurity diffusion region formed in said semiconductor substrate for surrounding said first and second impurity diffusion regions, and said first and second PN junction regions, and

a third electrode for grounding said third impurity diffusion region.

30. The diode as claimed in claim 19, further comprising an insulation region formed in said semiconductor substrate for surrounding said first and second impurity diffusion regions, and said first and second PN junction regions.

31. The diode as claimed in claim 19, wherein said insulation protection film comprises one of a localized oxidation of silicon film, a silicon oxide film and a silicon nitride film.

32. The diode as claimed in claim 19, wherein said

insulation protection film comprises a lamination film including at least two of a localized oxidation of silicon film, a silicon oxide film, and a silicon nitride film.

33. A diode comprising:

a semiconductor substrate;

an insulation protection film on said semiconductor substrate having m sets of three openings, each set of three openings being arranged in a predetermined direction, said three openings being spaced by two bridge portions having the same width in said predetermined direction;

m first impurity diffusion regions of a first conductivity type in a surface layer of said semiconductor substrate under center one of said three openings of each set;

2m second impurity diffusion regions of a second conductivity type in said surface layer under outer two of said openings of each set, respectively;

m sets of first and second PN junction regions in said surface layer, each set of said first and second PN junction regions are arranged between said first impurity diffusion region and said second impurity diffusion regions at both sides thereof, said first and second PN junction regions being covered with said bridge portions and having PN junction widths depending on said bridge portions, said insulation protection film having a melting point higher than the PN junction regions;

a first electrode on said insulation protection film connecting said m first impurity diffusion regions through

said openings; and

a second electrode on said insulation protection film connecting said 2m second impurity diffusion regions through said openings,

wherein m is a natural number more than one.

34. The diode as claimed in claim 33, wherein each of said openings has a rectangle shape of which longitudinal sides are defined by said bridge portions of said insulation protection film.

35. The diode as claimed in claim 34, wherein said longitudinal sides of said rectangle shape of said center one of said openings are different in length from said longitudinal sides of said outer two of said openings.

36. The diode as claimed in claim 34, wherein said openings of the insulation protection film have round portions or chamfered portions at its ends so that corners of said rectangle shape are rounded or chamfered.

37. The diode as claimed in claim 34, further comprising low impurity concentration diffusion regions in said surface layer covering end edge portions of at least one of said first and second impurity diffusion regions, wherein an impurity concentration of said low impurity concentration diffusion region is lower than an impurity concentration of said one of said first and second impurity diffusion regions, and wherein a conductivity type of said low impurity concentration diffusion region is the same as the conductivity type of said one of said first and second high impurity concentration diffusion regions.

38. The diode as claimed in claim 34, wherein said first and second electrodes have contact areas within said openings for contacting with said first and second impurity diffusion regions, a distance ($L_y$) between the transverse sides of said openings and contact areas is greater than a distance ($L_x$) between the longitudinal sides of said openings and contact areas.

39. The diode as claimed in claim 33, wherein said m sets of three openings in said insulation protection film are coaxially arranged.

40. The diode as claimed in claim 33, wherein said first electrode comprises a first lower layer electrode partially covering said first impurity concentration diffusion region inside said center one of said three openings, and said second electrode comprises second lower layer electrodes partially covering said second impurity diffusion region inside said outer two of said three openings, said diode further comprising an intermediate insulation layer on said first and second lower layer electrodes, said intermediate insulation layer having a first lower layer electrode opening at the corresponding position of said first lower layer electrode and second lower layer electrode openings at the corresponding positions of said second lower layer electrodes, wherein said first electrode further comprises a first upper layer electrode connected to said first lower layer electrode through said first lower layer electrode opening, and said second electrode further comprises a second upper layer electrode connected to said second lower layer electrodes

through said second lower layer electrode openings.

41. The diode as claimed in claim 40, wherein widths of said first and second upper layer electrodes is greater than widths of said first and second lower layer electrodes, respectively.

42. The diode as claimed in claim 40, further comprising a protection film on said first and second upper layer electrodes having first and second openings, wherein a first pad is formed by a part of said first upper layer electrode exposed through said openings and second pad is formed by a part of said second upper layer electrode exposed through said openings, and said first and second pads are provided on locations where said m sets of three openings are put therebetween, and widths of said first and second upper layer electrodes increase as distances to said first and second pads decrease, respectively.

43. The diode as claimed in claim 33, further comprising:

a third impurity diffusion region formed in said semiconductor substrate for surrounding said first and second impurity diffusion regions, and said first and second PN junction regions, and

a third electrode for grounding said third impurity diffusion region.

44. The diode as claimed in claim 33, further comprising an insulation region formed in said semiconductor substrate for surrounding said first and second impurity diffusion regions, and said first and second PN junction regions.

45. The diode as claimed in claim 33, wherein said

insulation protection film comprises one of a localized oxidation of silicon film, a silicon oxide film and a silicon nitride film.

46. The diode as claimed in claim 33, wherein said insulation protection film comprises a lamination film including at least two of a localized oxidation of silicon film, a silicon oxide film, and a silicon nitride film.

47. A diode comprising:

a semiconductor substrate;

an insulation protection film on said semiconductor substrate having n+1 openings arranged in a predetermined direction, said n+1 openings being spaced by n bridge portions having the same width in said predetermined direction, said n being a natural number more than one;

first and second impurity diffusion regions which are of first and second conductivity types, respectively, alternately arranged in a surface layer of said semiconductor substrate under said n+1 openings;

n PN junction regions having the same width under said n bridge portions in said surface layer between said first and second impurity diffusion regions, said n PN junction regions being covered with said n bridge portions and having the PN junction widths depending on said n bridge portions, said insulation protection film having a melting point higher than the PN junction regions;

a first electrode on said insulation protection film connecting said first impurity diffusion regions; and

a second electrode on said insulation protection film

connecting said second impurity diffusion regions.

48. The diode as claimed in claim 47, wherein each of said openings has a rectangle shape of which longitudinal sides are defined by said bridge portions of said insulation protection film.

49. The diode as claimed in claim 48, wherein said longitudinal sides of said rectangle shape of each of said openings for forming said first diffusion region are different in length from said longitudinal sides of said rectangle shape of each of said openings for forming said second diffusion region.

50. The diode as claimed in claim 48, wherein said openings of the insulation protection film have round portions or chamfered portions at its ends so that corners of said rectangle shape are rounded or chamfered.

51. The diode as claimed in claim 48, further comprising low impurity concentration diffusion regions in said surface layer covering end edge portions of at least one of said first and second impurity diffusion regions, wherein an impurity concentration of said low impurity concentration diffusion region is lower than an impurity concentration of said one of said first and second impurity diffusion regions, and wherein a conductivity type of said low impurity concentration diffusion region is the same as the conductivity type of said one of said first and second high impurity concentration diffusion regions.

52. The diode as claimed in claim 48, wherein said first and second electrodes have contact areas within said openings for

contacting with said first and second impurity diffusion regions, a distance ($L_y$) between the transverse sides of said openings and contact areas is greater than a distance ($L_x$) between the longitudinal sides of said openings and contact areas.

53. The diode as claimed in claim 47, wherein said n+1 openings in said insulation protection film are coaxially arranged.

54. The diode as claimed in claim 47, wherein said first electrode comprises first lower layer electrodes formed on said insulation protection film to cover said openings for forming said first impurity concentration diffusion regions and said second electrode comprises second lower layer electrodes formed on said insulation protection film to cover said openings for forming said second impurity diffusion region, said diode further comprising an intermediate insulation layer on said first and second lower layer electrodes, said intermediate insulation layer having first lower layer electrode openings at the corresponding positions of said first lower layer electrodes and second lower layer electrode openings at the corresponding positions of said second lower layer electrodes, wherein said first electrode further comprises a first upper layer electrode connected to said first lower layer electrodes through said first lower layer electrode openings, and said second electrode further comprises a second upper layer electrode connected to said second lower layer electrodes through said second lower layer electrode openings.

55. The diode as claimed in claim 54, wherein widths of said first and second upper layer electrodes is greater than widths of said first and second lower layer electrodes, respectively.

56. The diode as claimed in claim 54, further comprising a protection film on said first and second upper layer electrodes having first and second openings, wherein a first pad is formed by a part of said first upper layer electrode exposed through said openings and second pad is formed by a part of said second upper layer electrode exposed through said openings, and said first and second pads are provided on locations where said n+1 openings are put therebetween, and widths of said first and second upper layer electrodes increase as distances to said first and second pads decrease, respectively.

57. The diode as claimed in claim 47, further comprising:

a third impurity diffusion region formed in said semiconductor substrate for surrounding said first and second impurity diffusion regions, and said first and second PN junction regions, and

a third electrode for grounding said third impurity diffusion region.

58. The diode as claimed in claim 47, further comprising an insulation region formed in said semiconductor substrate for surrounding said first and second impurity diffusion regions, and said first and second PN junction regions.

59. The diode as claimed in claim 47, wherein said insulation protection film comprises one of a localized

oxidation of silicon film, a silicon oxide film and a silicon nitride film.

60. The diode as claimed in claim 47, wherein said insulation protection film comprises a lamination film including at least two of a localized oxidation of silicon film, a silicon oxide film, and a silicon nitride film.

61. A method of producing a diode comprising the steps of:

forming an insulation protection film on a semiconductor substrate;

forming three openings in said insulation protection film arranged in a predetermined direction, said three openings being spaced by two bridge portions of said insulation protection film having the same width in said predetermined direction;

ion-injecting first impurity into a surface layer of said semiconductor substrate through center one of said three openings to form a first impurity diffusion region of a first conductivity type;

ion-injecting second impurity into said surface layer through outer two of said openings to form two second impurity diffusion regions of a second conductivity type; and

forming first and second electrodes on said insulation protection film for connecting to said first diffusion region and for connecting said second diffusion regions, respectively.

62. The method as claimed in claim 48, wherein said insulation protection film comprises one of a localized oxidation of silicon film a silicon oxide film and a silicon

nitride film.

63. The method as claimed in claim 48, wherein said insulation protection film comprises a lamination film including at least two of a localized oxidation of silicon film, a silicon oxide film, and a silicon nitride film.

64. A method of producing a diode comprising the steps of:

forming an insulation protection film on a semiconductor substrate;

forming m sets of three openings in said insulation protection film, each set of three openings being arranged in a predetermined direction, said three openings being spaced by two bridge portions of said insulation protection film having the same width in said predetermined direction;

ion-injecting first impurity into a surface layer of said semiconductor substrate through center one of said three openings of each set to form m first impurity diffusion regions of a first conductivity type;

ion-injecting second impurity into said surface layer through outer two of said openings of each set to form 2m second impurity diffusion regions of a second conductivity type;

forming a first electrode on said insulation protection film connecting said m first impurity diffusion regions; and

forming a second electrode on said insulation protection film connecting said 2m second impurity diffusion regions,

wherein m is a natural number more than one.

65. The method as claimed in claim 64, wherein said

insulation protection film comprises one of a localized oxidation of silicon film, a silicon oxide film and a silicon nitride film.

66. The method as claimed in claim 64, wherein said insulation protection film comprises a lamination film including at least two of a localized oxidation of silicon film, a silicon oxide film, and a silicon nitride film.

67. A method of producing a diode comprising the steps of:

forming an insulation protection film on a semiconductor substrate having n+1 openings arranged in a predetermined direction, said n+1 openings being spaced by n bridge portions having the same width in said direction, said n being a natural number more than one;

ion-injecting first and second impurity into a surface layer of said semiconductor substrate through said openings to form first and second impurity diffusion regions of first and second conductivity type, respectively, to be alternately arranged in a surface layer of said semiconductor substrate under said n+1 openings; and

forming a first electrode on said insulation protection film connecting said first impurity diffusion regions; and

forming a second electrode on said insulation protection film connecting said second impurity diffusion regions.

68. The method as claimed in claim 67, wherein said insulation protection film comprises one of a localized oxidation of silicon film a silicon oxide film and a silicon nitride film.

69. The method as claimed in claim 67, wherein said insulation protection film comprising a lamination film including at least two of a localized oxidation of silicon film, a silicon oxide film, and a silicon nitride film.